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Broadband Low Reflection Surfaces with Silicon Nano-pillar Square Arrays for Energy Harvesting

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***Abstract*—In this work, optimization of the nanopillar arrays and thin films coated on silicon substrate has been investigated in order to minimize the optical reflection loss from the silicon substrate surface. Nano-pillars' height, incline angle, array properties are systematically optimized. Full field Finite Difference Time Domain method is used to simulate EM fields and calculate the reflection loss from the modified nanostructured substrate surfaces in 400nm-1100nm spectral range. Simulation optimization recipe for the nanopillar structure is clearly presented and it is not only useful for square arrays but for regular arrays of nano-pillars in general.**

Index Terms—**Nano-pillars, quantum efficiency, anti-reflection, thin films, nanostructures, truncated nano-cones, solar cells, solar energy.**

I. INTRODUCTION

GENERALLY CRYSTALLINE silicon based photonic devices such as photodiodes, solar cells, phototransistors need low surface reflectance over a wide spectrum of light in order to have high external quantum efficiency and energy harvesting through outer circuits. One of the conventional methods to reduce surface reflection is to use single layer dielectric at specific wavelength but this does not reduce reflectivity for broadband. SiO_2, SiN_x, TiO_2, Al_2O_3 dielectric materials are the most popular thin film materials for antireflection coatings. When double dielectric layers are used for this purpose, there are two reflection minimums in the reflection spectrum. Unfortunately, in order to achieve a broadband low reflection, multi-layer band pass filter should be used, but this requires many thin film layers, and this increases the production costs. However, this is not an optimum solution to the broadband low reflection problem. Surface modification is needed in order to obtain broadband low reflection from the optoelectronic substrate surfaces. This modification can be achieved by using micro [1] or nano-size [2-12] structures over the device surfaces. In order to build such small features, researchers used mainly wet etching and dry etching methods. For example, industrial pyramidal surface texturing for crystalline silicon uses anisotropic wet-etching method. In other methods, dry etching can be used with ionized gases in the plasma vacuum chambers. For some studies both etching methods are used in combination.

Some researchers studied some degree of randomness [9-13] in the periodic structures to decrease the reflection further. However, for large area applications this can have some advantages as well as disadvantages as to have some standard way of production.

Structure sizes show differences in these applications. Some applications use micrometer size pillars [1] and some applications use nano-meter size pillars. For applications that need thin silicon film layers, nanometer size structures have to be used in order to achieve low reflection in broadband. If the pillars are tall (more than micron) then this can lead to quantum efficiency loss due to charge recombination in the pillar structure and the generated electron hole pairs cannot be extracted from the devices for energy harvesting. Therefore, the height of the pillars should be optimized to get low reflectivity. When the height of the pillars is too short then the coupling of incident light into the silicon substrate is low.

To summarize, recently several types of surface nanostructures have been investigated. Moth-eye nano-pyramidal pillars which use graded index refractive index to reduce reflection. Nanowires and nanocylinders that use Mie resonances (scattering) which result in overall decrease in reflection. Metallic nanoparticles use their plasmonic effect to direct electromagnetic energy through the substrate effectively and decrease the reflection from the surface.

Optimization studies of the nanostructured surfaces in optoelectronic devices are still popular since the energy sector is very crucial for the economy of the countries. Even one percent increase in energy efficiency in solar cells means millions of dollars saving in countries' economies. In order to obtain high efficiency in solar cells, low reflection from the surfaces irrespective of incident angles in wide wavelength spectrum is needed.

In this work, we optimized nano-pillars filling ratio, pillar height, apex angle, and calculated the weighted average reflection with respect to wavelength to get the overall efficiency improvement for the optoelectronic devices. We focused on nano-pillar arrays of square type.

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II. Methods and Simulation Results

In this letter, we present the optimization of the nano-pillar square arrays in order to achieve broadband low reflection surfaces. When compared to a bare planar crystalline silicon wafer surface, the modified surface has significant reduction in reflection in 400nm-1100nm range.

We used Finite Difference Time Domain (FDTD) method to simulate photonic nanostructures. We placed monitors just below the nano-pillars to calculate the transmission to the bulk substrate. We also placed a monitor above the structure to simulate the EM fields and calculate the reflected power. We also calculate the light absorbed in the nanostructure. The optical constants of crystalline structure and thin films are taken from [14]. We first optimized the filling ratio of the nano-pillar arrays, then height to minimize the reflection. We also varied the pillar wall angle to create truncated cones to search the effect of cone structure to the reflection properties. We used dielectric anti-reflection coatings with SiO_2 thin film to decrease the reflection further. These nano-cone truncated pillar structures can be fabricated using e-beam lithography and dry etching techniques. Due to the nature of etching processes, the vertical pillars can be obtained under special physical and chemical conditions [17, 18]. It is important to have vertical pillars to get optimum reflection from such structures since as the pillar angle gets lower, the reflection start to increase Fig.7. For large area applications, nano-imprint lithography can be used with a previously prepared template using nano-fabrication methods. We also realized that to increase the efficiency of photonic devices, we have to increase the optical power absorbed in the bulk of the active silicon layer. The absorbed light in the nanostructures part could be lost due to recombination and cannot contribute to the photocurrent with large percentage. Therefore, we have to maximize the absorption not in the nanostructures but the optical absorption in the bulk silicon active device region.

Solar irradiance differs with wavelength. We can use the total reflection of light from the surface weighted with solar irradiance. This way the performance of the low reflection loss performance can be quantified better. ASTM Air Mass 1.5 direct solar irradiance is used for the calculation. In this formulation, irradiance is multiplied with the wavelength and the integral is taken with wavelength. The numerator is composed of Irradiance multiplied with wavelength and reflection. For a random polarization condition, both TE and TM polarizations are calculated, and the average is taken to get more realistic result. We used the formula given in Equation (1) in calculating the weighted averaged reflection in 400nm-1100nm wavelength range.

The novelty of our study is the following: 1) Instead of sweeping mode of the simulation, we optimized the parameters in sequence and each time, the optimization is done with respect to one parameter. This saves computational time. 2) We checked whether the angle of incline effects the reflection properties. 3) The optimization is done in terms of filling ratio, height, pillar angle, and dielectric anti-reflection coating thickness. 4) We obtained the lowest averaged reflection loss for regular square array of silicon nanopillars.

As a first step, we fixed the diameter of the pillars as **d**=190nm and pillar height as **h**=120nm and varied the ratio of pillar diameter to period of pillar a which is **d/a** and varied that from 0.4 to 1.0. Minimum weighted averaged reflection is obtained as 3.91 percent at **d/a**=0.7 as depicted in Fig. 2. We used **a** to denote the period of the square nano-pillar array. Since we are dealing with the thin film device applications, we take the height range 60nm-190nm since larger and smaller height nano-pillar arrays have high reflectivity in the interested spectral region. As depicted in Fig.3, and Fig.4, we varied the height of the pillars and we found that 120nm is the optimum height especially for low reflection in 400nm-1100nm range. For large pillar heights, the reflectivity increases especially for UV region in the spectrum. For shorter pillars, the reflection increases especially for wavelengths larger than 600nm. The weighted averaged reflection calculations for the whole set of height range can be seen in Fig.4. Therefore, we fixed the pillar height at 120nm.

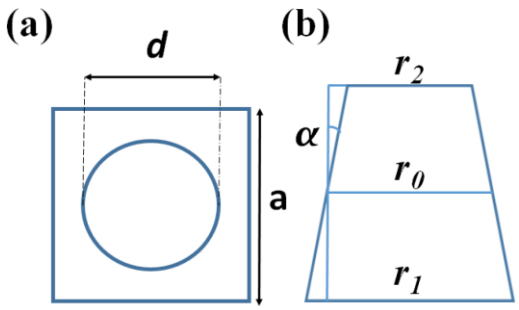

Fig.1. (a) Unit cell used in the simulation of square nanopillars, (b) Cross section of truncated pillar structure to define the pillar angle

$$Weighted\ Average\ Reflection = \frac{\int_{400}^{1100} \frac{R_{TE}(\lambda) + R_{TM}(\lambda)}{2} I(\lambda)\lambda d\lambda}{\int_{400}^{1100} I(\lambda)\,\lambda d\lambda} \quad (1)$$

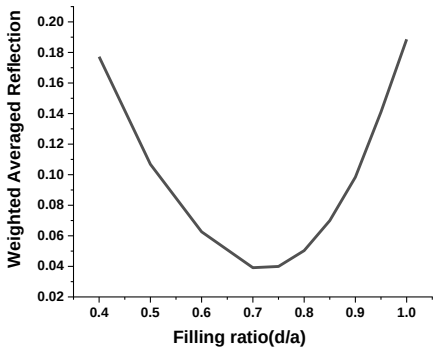

Fig.2. Weighted averaged power versus filling ratio of the pillars

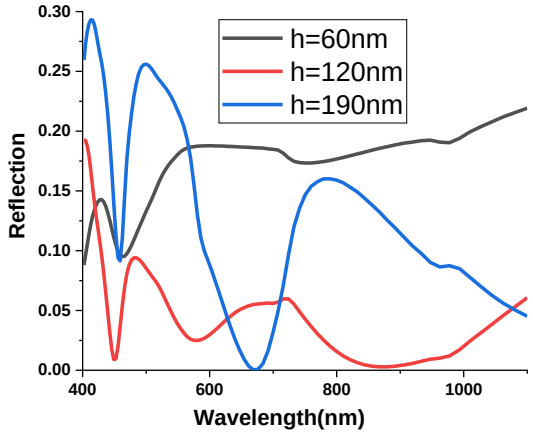

Fig.3. Height optimization of the pillars

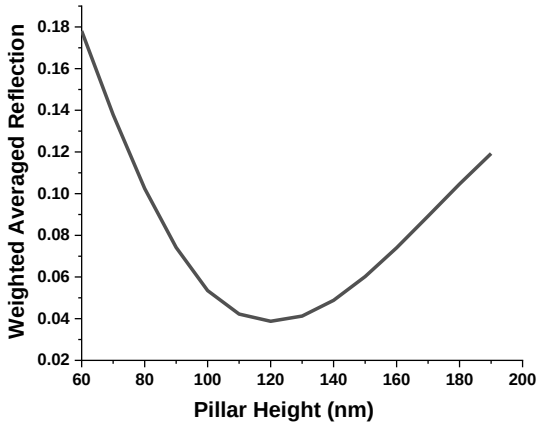

Fig.4. Weighted Averaged Reflection versus Pillar height

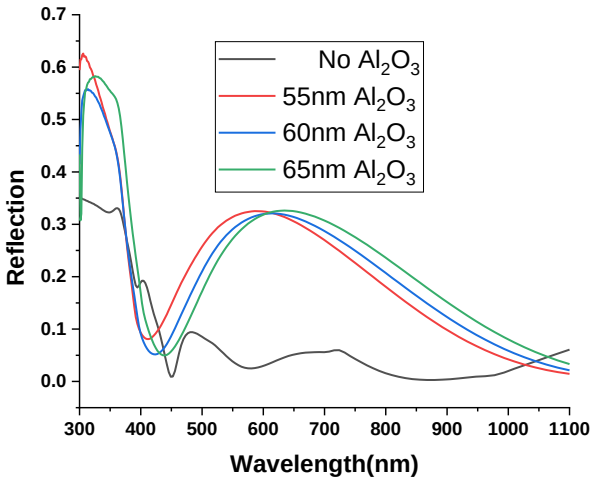

Fig.5. Anti-reflection dielectric Al_2O_3 thin film coating on the nanopillar array

We further examine the anti-reflection dielectric film Al_2O_3 coating. In figure 5, 55nm, 60nm, and 65 nm thick Al_2O_3 thin film added at top of the nano-pillar structures. As can be noticed, the reflection is minimum and small in about 50nm range around the minimum [15]. At other spectral wavelength range 400nm-1100nm, the reflection is even larger than we obtained when only nano pillar arrays are used Fig.5. Therefore, instead of using the concept of antireflection minimization at one point, the analysis of a range of thin film thickness is needed using FDTD simulations.

As depicted in Fig.1(b), the truncated cone architecture is used to decrease furher the reflection from the surface. The angle at which the pillar walls make with the vertical varied between 0-26 degrees. As can be seen in Fig.6, for wavelengths below 550nm, the reflection decreases with pillar slope however above 550nm, the reflection increases considerably. Truncated nanopillars apex angle can be achieved with optimizing the dry etching conditions, e.g., chamber pressure, temperature, gas flow rates. When the weighted average reflection is calculated for different pillar slopes (delta r is the difference of the bottom and top truncated nanocone pillar diameters) as shown in Fig.7. The minimum weigted averaged reflection occures for vertical pillars therefore it is very important to obtain vertical pillars in square nanopillar arrays to obtain minimum reflection surfaces. For wavelengths smaller than 550nm, truncated nanocone arrays have lower reflections. However, for wavelengths larger than 550nm, they have higher reflections. For specific range of wavelengths, this property can be useful.

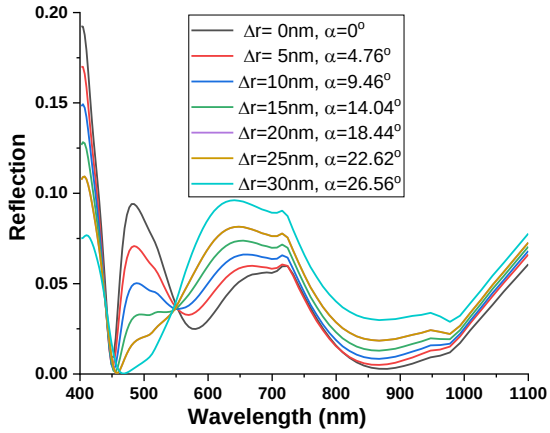

Fig.6. Reflection optimization with cone angle alpha.

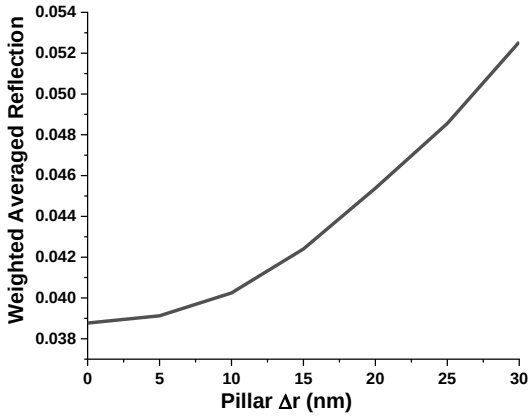

Fig.7. Total weighted reflection with solar irradiance on earth surface versus pillar angle.

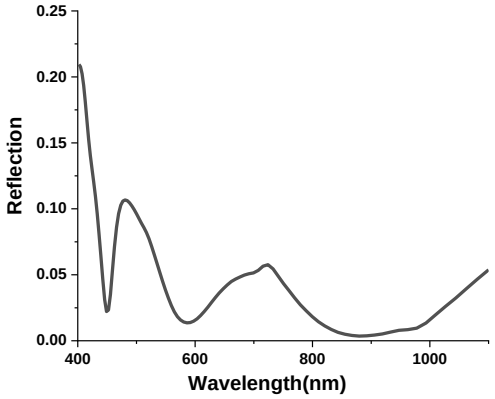

Fig.8. The optimum structure reflection versus wavelength with 5nm SiO_2 thin film.

It is also noticeable that the reflection is relatively high for the UV spectral region below 450nm wavelength. This is due to the fact that at small wavelengths the light rays start to ignore the nano-pillar array structure and get reflected from the bare silicon substrate surface. Therefore, reflection loss is high for UV region. Dielectric anti-reflection coating is also investigated by depositing SiO_2 layer on top of the all structure with thicknesses varied from 5nm to 70nm. The minimum reflection is obtained with weighted averaged reflection of 3.75 percent with 5nm thickness in 400nm-100nm range which is one of the lowest reflection losses reported in the literature. The reflection spectra is depicted in Fig.8. When we compare the recent results from other groups, the lowest value for the average reflection from regular nanopillar square arrays is 4 % Table 1. This averaged reflection loss can be avoided further if compound nano-pillars with a scattering tip on top of the pillar are used so that light can be absorbed in the substrate not in the pillar structures. The absorption in the UV region of the spectrum at the nano-pillar array structure is large; this is also a big issue if there is recombination in the nanostructure for energy extraction from an active device. We will pursue these issues in future work.

TABLE I
COMPARISON OF RECENT RESULTS FOR THE AVERAGE REFLECTIONS FROM REGULAR SQUARE NANOPILLAR ARRAYS

Author	Year	R (Average)
J. Li et al. [19]	2009	>10 %
C. Lin et al. [20]	2011	4.64 %
J. Proust et al. [21]	2016	4 %
J. Kim et al. [22]	2021	7.1%

III. Conclusion

The reflection properties of the nanostructured silicon surfaces have been investigated and understood physically through weighted average reflection as a function of wavelength. We see that using truncated nano-cones has potential to reduce further the total weighted reflection loss from the surface of the photonic devices surfaces for specific wavelength range. For broadband low reflection, vertical nano-pillars should be used for square pillar arrays. We developed a simulation recipe to achieve minimum weighted average reflection architecture of the structure with respect to pillar height, filling ratio, incline angle, dielectric anti-reflection coating. Depositing 5nm SiO_2 thin film, one of the minimum reflections is obtained for square array type nano-pillar structures in the literature, which is 3.75 %. In order to optimize nanopillar structure further, adding a scattering tip structure on top of the pillars will be investigated as future study.

These modified nanostructured surfaces concept is useful for photonic device applications having thin film silicon or active absorbing semiconducting material for optical energy harvesting through low surface reflection over a broadband optical spectrum [16]. In broad sense, thin film solar cells, photodetectors, phototransistors applications are the potential applications of these nanostructured surfaces with low reflection.

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BIOGRAPHIES

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