Selective Remanent Ambipolar Charge Transport in Polymeric Field-Effect Transistors For High-Performance Logic Circuits Fabricated in Ambient

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Solution-processable polymer semiconductors are promising for low-cost device fabrication, mechanical flexibility, and tunable optoelectronic properties.[1] Logic circuits based on polymer semiconductors are expected to open new possibilities for plastic electronic applications including flexible displays, printable radio frequency identification (RFID) tags, and large-area sensors.[2] To this end, organic field-effect transistors (FETs) based on polymer semiconductors have been studied extensively over the last decade, and recent efforts in molecular design and device architectures have resulted in tremendous performance progress for unipolar operation, with charge carrier mobilities reaching or even exceeding that of amorphous silicon (~0.5–1.0 $cm^2\ V^{-1}\ s^{-1}$).[3] Furthermore, great efforts have been invested in developing dual unipolar component systems, e.g. for complementary circuits. Nevertheless, such bulk-heterojunction blends typically suffer from phase separation issues.[4,5] Ambipolar polymer semiconductors, in which both hole- and electron-transporting functions are attained in a single semiconductor, do not suffer from this limitation. For this reason ambipolar semiconductors are promising candidates for simple and low-cost fabrication of organic logic circuits.[6] However, very few ambipolar polymers are known to work in ambient, and they typically show modest electron/hole mobilities (~10^{-4}–10^{-2} $cm^2\ V^{-1}\ s^{-1}$),[7,8] while higher ambipolar mobilities of ~0.1–1.0 $cm^2\ V^{-1}\ s^{-1}$ are only reached under nitrogen.[9]

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DOI: 10.1002/adma.201403070

The design of circuits employing organic complementary metal oxide semiconductor (CMOS) architectures requires the development of both p-channel and n-channel semiconductors with high performance and air-stability.[10] The advantages of this approach as compared to unipolar logic circuits are low power dissipation, relatively higher operating frequencies, good noise margin, and overall robust operation.[11] However, organic ambipolar complementary circuits still face a few issues, including unbalanced field-effect mobility (μ) and asymmetric threshold voltage (V_{TH}) for holes and electrons as well as the difficulty in achieving efficient hole and electron injection from the same source electrode material. These shortcomings result, for instance, in asymmetric voltage-transfer characteristics of the corresponding inverters. Recently, several approaches have been reported to overcome these challenges by optimizing the molecular design for well-balanced values of hole and electron mobilities,[12,13] introducing an interlayer for efficient charge injection,[14] and engineering the gate dielectric interface.[15] For example, dielectric layers comprising a blend of fluorinated high-k insulating polymer and conventional (non-fluorinated) low-k polymers, such as polystyrene (PS) and/or poly(methyl methacrylate) (PMMA), have been used to induce a desired balance in the ambipolar characteristics of a predominantly n-type semiconductor with consequently high inverter performances.[16] This result was achieved because the high-k fluorinated dielectric polymer enables enhanced accumulation of holes at the semiconductor/dielectric interface, by bending the semiconductor energetic levels.

In order to further simplify the device manufacturing process and to make integration easier, reconfigurable circuits are required alongside the development of new high-performance organic ambipolar materials. In this respect, programmable and bistable switching organic ferroelectrics lead to potential applications in reconfigurable systems. Fluorinated ferroelectric polymers, such as poly(vinylidenefluoride-*co*-trifluoroethylene) (P(VDF-TrFE)), show a remanent polarization. In P(VDF-TrFE) the molecular dipole moments reside perpendicular to the backbone of the material and are defined by the difference in electronegativity between the hydrogen-substituted carbons and the fluorine-substituted carbons. The dipoles are then aligned collectively by the application of an electric field. This causes rotation of the monomer groups of crystalline P(VDF-TrFE) domains, which gives rise to the ferroelectric response of this material.[17] Such effect has been used to fabricate FET-based memories.[18] In this type of devices the memory effect arises from the modulation of the surface

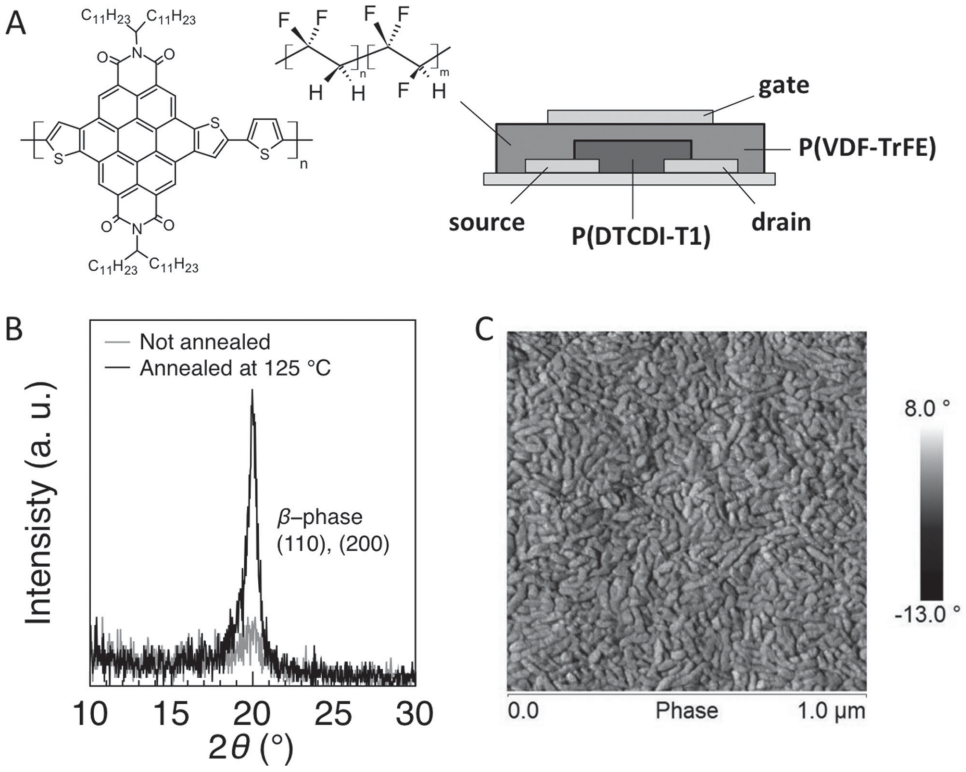

Figure 1. (a) Molecular structures of P(DTCDI-T1) and P(VDF-TrFE) along with the schematic layout of the ferroelectric polarization-enhanced ambipolar transistor. (b) XRD pattern of a 200-nm-thick P(VDF-TrFE) film before (gray) and after (black) annealing at 125 °C. (c) AFM phase image of the annealed P(VDF-TrFE) film.

charge density in the semiconductor by the remnant polarization of the ferroelectric gate insulator. The typical fingerprint of ferroelectric dipoles switching in ferroelectric FETs (FeFETs) is a sharp change of the channel conductance at the coercive field of the ferroelectric gate and has been clearly observed for solution-processed polymer FeFETs including a p-type unipolar semiconductor layer.[19,20] Here, it was shown that the induced surface-charge density has a relatively higher value (larger than 15 mC m^{-2}) as compared to what is found for FETs gated via conventional dielectrics.[19] Thus, the simplified manufacturing process deriving from the use of ambipolar polymers and the easy programmability of organic ferroelectric insulators would allow for efficient, reconfigurable CMOS-like circuits.

In this study we demonstrate selective remanent ambipolar charge transport in polymeric FETs operable in ambient conditions. The channel polarity of FETs based on an ambipolar dithienocoronenediimide-thiophene copolymer can be permanently switched into a p- or n-type mode using the remanent polarization of the ferroelectric gate insulator. The extremely high charge carrier density (15–20 mC m^{-2}) induced by the ferroelectric polarization is the origin of the high drain currents (10^{-6} A) observed at low source-drain voltages (5 V). This result is in contrast to FETs where conventional dielectric gate insulators are used. Such ferroelectric polarization-enhanced FETs are exploited here to enhance the performance of complementary-like inverters, and nondestructive read-out operation, CMOS-like compatible one transistor-one transistor (1T1T) memory cells.

Top-gate bottom-contact FETs were fabricated with a recently discovered ambipolar dithienocoronenediimide-thiophene copolymer (P(DTCDI-T1))[8] as the semiconducting layer (**Figure 1**a). This device architecture is chosen due to the superior injection characteristics of the staggered device geometry and to avoid interface issues caused by the surface roughness of P(VDF-TrFE) layer. Additionally, the top ferroelectric insulator layer provides an encapsulation for the underlying semiconductor, making the devices operation more stable in ambient conditions. For device fabrication, the semiconductor thin film (~50 nm thick) was spin-coated on untreated gold source-drain electrodes/glass substrates from solution (8 mg mL^{-1} in dichlorobenzene). Next, the polymeric dielectric P(VDF-TrFE) layer (40 mg mL^{-1} in diethyl carbonate) was spin-coated. These films were annealed at 125 °C prior to thermal evaporation of the gold gate electrode, in order to enhance the crystallinity and thus the ferroelectric properties of P(VDF-TrFE). X-ray diffraction (XRD) analysis for a 200-nm-thick P(VDF-TrFE) film shows the (110) and (200) ferroelectric β-phase peak at ca. 20° in the diffraction angle (Figure 1b). Annealing at 125 °C produces a more intense diffraction peak, indicating a higher degree of crystallinity.[21] Atomic force microscopy (AFM) phase image of the annealed films confirms the typical rod-like features of the β-phase P(VDF-TrFE) surface (Figure 1c), with a crystalline grain width of 20–40 nm (see Supporting Information Figure S1 for the topography image). All device processing and electrical measurements were carried out in ambient atmosphere except for the gate electrode deposition and film drying steps (see Experimental Section for further details).

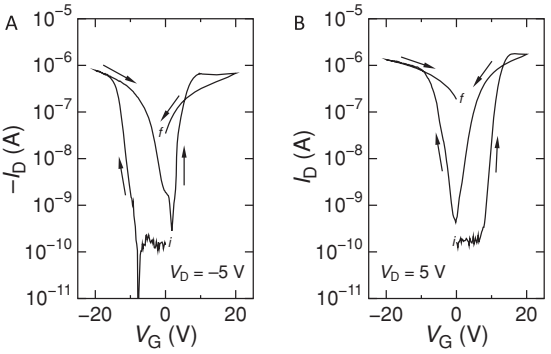

Figure 2. Representative transfer curves of the ambipolar P(DTCDI-T1)-based FET operating in hole (a) and electron (b) accumulation. The initial (*i*) and final (*f*) current states are clearly indicated in the graphs. In the FeFET the ferroelectric layer thickness is 200 nm.

The current-voltage characteristics of a representative ambipolar polymer FET are shown in **Figure 2**. The transistor (W/L = 1 mm/50 µm) operates in the accumulation mode with the transfer curves exhibiting a typical "butterfly" shape for both the p-channel (Figure 2a) and the n-channel (Figure 2b) operations. This is consistent with the current retention behavior due to the ferroelectric polarization. In fact, when the polarization switches from one state to the other, charges are displaced across the ferroelectric layer. The associated switching currents appear as sharp features in the drain current at a coercive voltage (V_c) of around ±10 V (E_c = 50 MV m^{-1} for the 200-nm-thick P(VDF-TrFE) annealed at 125 °C.[21] Their presence and voltage level confirms that ferroelectric polarization switching drives the observed current hysteresis effect, rather than traps and/or fixed charges in the dielectric layer. The switching voltage is found to be independent of the device channel length. Before the very first sweep (V_G = 0 V), the P(VDF-TrFE) film is unpolarized and the drain current is as low as 0.1 nA. Upon increasing the negative (positive) gate bias beyond the coercive voltage, the ferroelectric film fully polarizes and holes (electrons) are accumulated in the FET channel. Interestingly, the drain currents both in the p- and the n-mode are nearly identical, indicating that the charge density is similar for both modes of operation in these devices. We note that the hole mobility of P(DTCDI-T1) FETs when non-ferroelectric dielectrics are used as gate insulators (e.g., PMMA), is typically one order of magnitude lower than the electron mobility.[8] The balanced ambipolarity, with respect to the mobility, in the ferroelectric polarization-enhanced FETs is likely attributed to the effect of the ferroelectric dipoles in the fluorinated P(VDF-TrFE), which enhances the positive charge carrier density in the channel.[16] The charge transport mobility derived from the transfer characteristics in the linear regime approaches 0.1 cm^2 V^{-1} s^{-1} for both holes and electrons, being the highest balanced mobility for devices measured in ambient.[13] As a comparison to a widely studied polymer for which transport has been modulated from n- to p-type using several approaches,[14,16,22] we investigated the charge transport of the naphthalene-bis(dicarboximide)-dithiophene polymer P(NDI2OD-T2). While switching is observed depending on the dielectric polarization, the predominantly electron transport characteristics of P(NDI2OD-T2) prevent to achieve well balanced electron and hole currents (Figure S2).

The device response of P(DTCDI-T1)-based FETs is found to be stable even after 3 months of storage in ambient atmosphere (Figure S3), with only a minor degradation of the *I-V* characteristics (I_{on} from 10^{-6} A to 10^{-7} A). Importantly, such performance deteriorations are reversible as observed by re-testing the same devices under vacuum (Figure S4), indicating an exceptional stability of P(DTCDI-T1) to the ambient trapping species (O_2 and H_2O). Thus, these devices should be easily stabilized by using a conventional passivation layer. These values of electron mobilities compares favorably with those reported in the saturation regime ($|V_{DS}|$ = 60 V) by using PMMA as the gate insulator.[8] It is also noteworthy that the use of a single ambipolar polymeric layer, instead of a dual unipolar component system such as the one formed from an interpenetrating network of semiconductors, circumvent phase separation issues.[5] Previous attempts to realize ambipolar FETs based on heterogeneous semiconductor blends and a ferroelectric-functionalized bottom gate dielectric have shown indeed that morphological differences between the pure semiconductors and the interpenetrating network affects the charge carrier mobility of the single components.[23]

Although the drain currents in the off-state (V_G = 0 V) and on-state ($|V_G|$ = 20 V) differ more than a factor of 10^4, the drain-current on/off ratio at V_G = 0 V (defined as the ratio of the drain currents at the final and initial state of the voltage cycle) differs typically by only 2 orders of magnitude or higher at the very first sweep for all devices we measured, and reduces to less than 10 when the device is swept further (Figure S5). Similarly low on/off ratios at zero V_G have been reported for ambipolar FeFETs based on a semiconductor blend and is ascribed to the accumulation of both charge carriers in the channel.[23] Small shifts in the V_{TH} are also observed and contribute to slightly reduce the transistor current. This is attributed to charge trapping at the semiconductor-ferroelectric interface.[24] Measuring the FETs in vacuum reduces the threshold voltage shifts and transistor current degradation. Interestingly, it should be noticed that if two consecutive unipolar voltage sweeps are applied to the ferroelectric layer, only the first sweep contributes to the ferroelectric dipoles switching. Thus once programmed, the device operates as either a p-type or an n-type FET. This results in a marked reduction of the drain current hysteresis, as shown in **Figure 3**. In fact the hysteresis voltage window, defined as the voltage

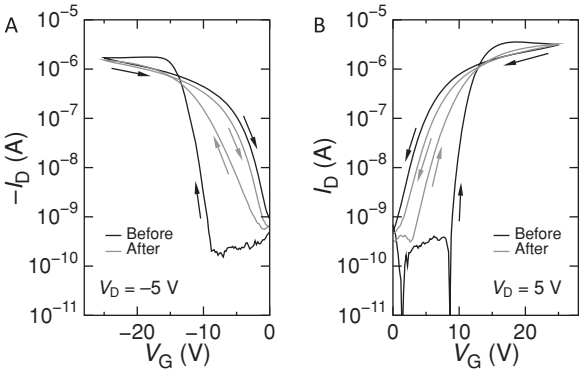

Figure 3. Transfer characteristics of the ambipolar P(DTCDI-T1)-based FET operating in hole (a) and electron (b) accumulation before (black solid line) and after (gray solid line) polarization of the ferroelectric dipoles.

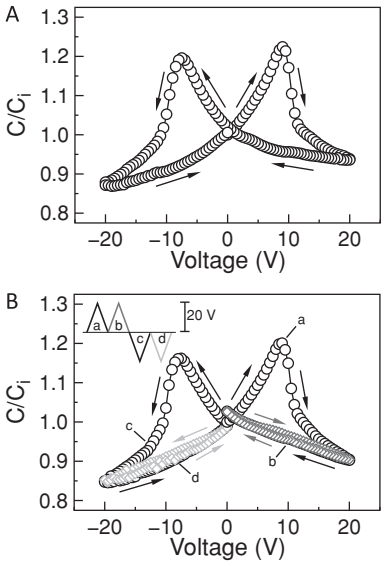

Figure 4. (a) Normalized capacitance-voltage measurement of a metal-insulator-semiconductor (MIS) structure with a 200-nm-thick ferroelectric P(VDF-TrFE) gate dielectric. (b) Programming the ferroelectric layer with two consecutive unipolar voltage loops (see inset) results in a loss of hysteresis.

difference at $I_D = 10^{-8}$ A, reduces from approximately 9 V to less than 2 V. Hysteresis reduction is also visible in the I_G-V_G characteristics, as the displacement current typically appears as a peak in the gate current (see Figure S6).

Capacitance-voltage (*C-V*) measurements offer the opportunity to measure and distinguish between accumulation and polarization of different charged species at the insulator-semiconductor interface. The typical *C-V* characteristic of a P(DTCDI-T1)-based metal-insulator-semiconductor capacitor (MIS) including a 200-nm-thick P(VDF-TrFE) gate dielectric is presented in **Figure 4**a. The normalized *C-V* curve shows a clear non-linearity and a "butterfly-shaped" hysteresis for both negative and positive biases. The hysteresis originates from the switching between the two states in which the ferroelectric gate insulator is polarized. This behavior is also reported for P(VDF-TrFE)-only capacitors and originates from the bias-field-dependent permittivity of P(VDF-TrFE).[25] The change of polarization of the insulator leads to a peak in the capacitance when the coercive field is reached. For a 200-nm-thick P(VDF-TrFE), this transition point is expected to appear at ±10 V. The surface charge density (ρ) of the on-state for both holes and electrons can be estimated from the *C-V* measurement data given in Figure 4a. Integrating the capacitance over the voltage in fact leads to a ρ value of 15–20 mC m^{-2}. This rather high remanent surface-charge density is induced by the ferroelectric polarization and compares favorably with previously reported values found in unipolar FeFETs.[19] The induced surface-charge density has a higher value as compared to what is obtained with conventional dielectrics[19] and results in the high drain current found already at low source-drain voltages. Hence, the *C-V* curve presented in Figure 4a strongly confirms that field-effect accumulation of both electrons and holes occurs in P(DTCDI-T1) and is controlled and gated by the ferroelectric switching of P(VDF-TrFE). For comparison, the *C-V* characteristics of a MIS capacitor where a unipolar polymer serves as the semiconducting layer show an asymmetric capacitance bistability with a marked transition from a high-capacitive state (accumulation) to a low-capacitive state (depletion).[20,26] Thus, the state of polarization of the ferroelectric insulator, included in a MIS capacitor, may be determined from the appearance of the maxima in the *C-V* plot. Consequently, as discussed before for the ferroelectric polarization-enhanced FET transfer characteristics, the *C-V* curves reported in Figure 4b do not display the same degree of hysteresis for two consecutive unipolar voltage loops (see inset to Figure 4b). On the initial sweep to positive (or negative) voltages, the capacitance plots exhibit broad maxima as in Figure 4a. The return sweep and subsequent unipolar sweeps show only the underlying behavior with essentially constant capacitance for both positive and negative accumulation voltages. These results clearly point out that the polarity of the channel can be permanently switched from p-type to n-type and back, depending on the polarization state of the ferroelectric dielectric.

A crucial step towards realizing robust and low power circuits is the use of complementary logics, where reliable n-type as well as p-type FET operation is essential. For this purpose the precise control of the polarity in P(DTCDI-T1)-based FETs through a proper programming of the gate dielectric can be utilized to realize balanced, high-performance complementary inverters. The fabricated inverters are based on a complementary-like design as depicted in the circuit layout of **Figure 5**a, where one FeFET is programmed to work as a p-type (*p*, pull-up transistor) and the other FeFET is programmed to operate as an n-type (*n*, pull-down transistor). The resulting inverter characteristics are shown in Figure 5b ($W_p/L_p = W_n/L_n$ = 10 mm/10 µm). When the supply voltage (V_{DD}) is set to +10 V and the input voltage (V_{IN}) is swept from 0 to $V<V_c$, a relatively high gain value, larger than 16, is obtained (see inset to Figure 5b). Here, gain is defined as dV_{OUT}/dV_{IN}. Note that the ferroelectric thickness limits the supply voltage as well as the input voltage of the inverter. In fact, when an input voltage larger than the ferroelectric coercive voltage is applied, it results in instability of the ferroelectric polarization and consequent worsening of the inverters characteristics. The switching voltage of the inverter ($V_{OUT} = V_{IN}$) is about the ideal $V_{DD}/2$ = +5 V, since the ambipolar charge transport is almost perfectly balanced. Complementary-like inverters, based on ambipolar semiconductors, typically display a characteristic Z-shaped output voltage due to parasitic currents running along the channel. This is because the FETs cannot be switched off completely.[27] This leads to a loss in output voltage due to leakage currents. Note that this effect is greatly reduced in our devices and it is only found for very low input voltages (that is, V_{IN} close to 0 V). Here, a parasitic current exists and is likely due to instability in the pull-down transistor that can cause slight depolarization of the ferroelectric insulator. The so-called worst-case noise margin (NM) is found by mirroring input and output voltages in the V_{OUT} versus V_{IN} graph and by determining the size of the maximum square that fits between the original and mirrored transfer curves, as shown in Figure 5b.[28] The inverters exhibit a noise margin of 3.2 V at V_{DD} = +10 V. The latter is approximately 65% of its maximum theoretical value (at V_{DD} = +10 V) given as $NM_{max} = V_{DD}/2$ = +5 V. These values are substantially

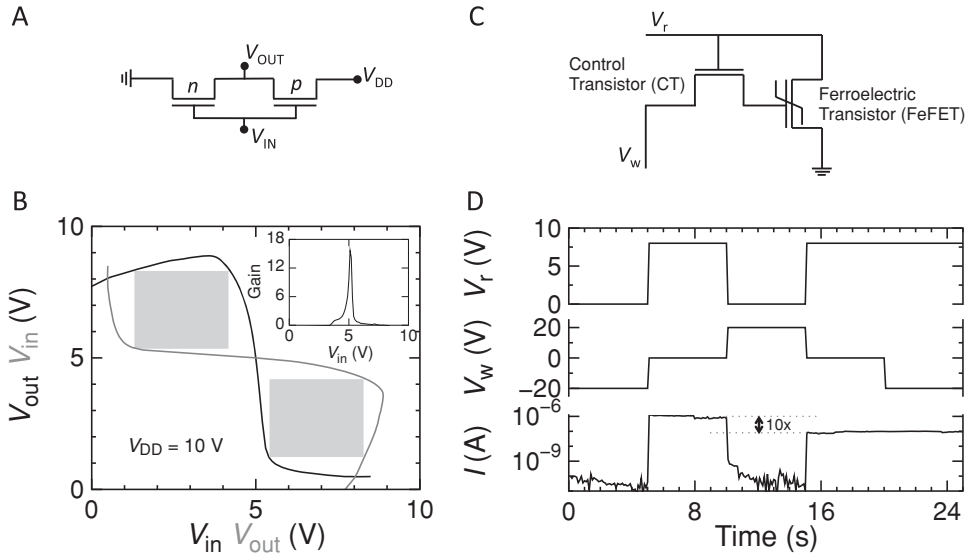

Figure 5. (a) Schematic representation and (b) input-output characteristics with worst-case noise margin extraction of a complementary-like inverter comprising ambipolar FETs. The inset shows the gain defined as dV_{OUT}/dV_{IN}. (c) Schematic representation of the 1T1T memory cell and the corresponding electrical characteristics (d).

larger than those reported for p-MOS inverters used in complex circuitry and among the best based on solution-processed organic CMOS-like inverters operating at such a low supply voltage (V_{DD} = +10 V).[28,29] Thus, both the gain and NM values for our complementary-like inverters suggest that our ambipolar-based technology is suitable for implementation in digital logic circuits.

Finally, we demonstrate that the memory functionality deriving from the remanent ferroelectric polarization in these ambipolar FeFETs can also be exploited to store information in a typical 1T1T memory cell (Figure 5c-d). We chose to work with this architecture due to its non-destructive readout operation and full compatibility with CMOS technology.[30] The control transistor (CT) comprises P(DTCDI-T1) as the semiconductor layer and PMMA as the dielectric (non-ferroelectric) layer. The CT is connected by external wiring to the P(DTCDI-T1)-based FeFET as represented in Figure 5c ($W_{CT}/L_{CT} = W_{FE}/L_{FE}$ = 500 µm/30 µm). When the reading voltage (V_r) is set to zero and the writing voltage (V_w) is –20 V, writing is enabled and a very low read-out current can be measured because of the lack of a V_{DS} at the FeFET (Figure 5d). Then, V_r is biased at +8 V and a read-out current is now measured, corresponding to the on-state of the FeFET. A tenfold lower read-out current is measured after poling the ferroelectric gate dielectric at V_w = +20 V (that is, off-state). The difference in on-state and off-state current reflects the low on/off ratio observed for the ambipolar FeFETs discussed before. Remarkably, the operation of the cell is not affected by the change in V_w under reading conditions (V_r = +8 V), demonstrating the reliability of the memory cell.

In conclusion, we demonstrated high-performance air stable ambipolar polymeric FETs with a programmable polarity. The polarity of the channel can reversibly be switched from p-type to n-type operation, depending on the polarization state of the ferroelectric insulator. Due to the remanent polarity, our device architecture is suited as a building block in complementary logic circuits, where well-balanced p- and n-type characteristics are needed, or in CMOS compatible 1T1T memory cell for non-destructive read-out operation.

Experimental Section

Materials: P(DTCDI-T1) was synthesized according to a previously published procedure[8] and used as received. P(NDI2OD-T2) was supplied by Polyera Inc. (ActivInk N2200) and used as received. The semiconductors were dissolved in 1,2-dichlorobenzene (8 mg mL^{-1}) and filtered with a 0.2 µm polytetrafluoroethylene (PTFE) syringe filter. P(VDF-TrFE) (70/30 mol%) was purchased from Solvay SA and used as received. P(VDF-TrFE) was dissolved in diethyl carbonate (DEC) at a concentration of 40 mg mL^{-1} and filtered through a 0.1 µm filter. PMMA (M_w = 120 kDa) was dissolved in 2-butanone (MEK) at a concentration of 70 mg mL^{-1}. Thin films were prepared by spin-coating in a class 1,000 clean room environment.

Device Fabrication and Characterization: A 50-nm-thick semiconductor layer was spin-coated at 1500 rpm for 120 s on corning glass substrates with photolithographically patterned source/drain electrodes (3-nm-thick Ti and 27-nm-thick Au). The films were then annealed at 120 °C for 1 h under N_2. Next, the P(VDF-TrFE) solution was spin-coated on top of the semiconductor layer and annealed at 125 °C for 15 min in vacuum oven to increase the film crystallinity. The P(VDF-TrFE) film thickness was measured by ellipsometry and confirmed by using a DekTak profilometer. For the 1T1T memory cell, PMMA solution was spin coated on top of the semiconductor layer and annealed at 120 °C for 1 h on a hot plate in a N_2 atmosphere. Finally, an 80-nm-thick Au gate electrode was thermal evaporated on top of the dielectric layer.

The transistor performances were characterized using a semiconductor parameter analyzer (Keithley 4200-SCS), while the impedance measurements were carried out with an Alpha high-resolution dielectric analyzer (Novocontrol GmbH). For the latter, an AC voltage of 0.3 V was applied at the frequency of 100 Hz. A DC voltage was swept from positive to negative voltages. We used an equivalent circuit model made of a resistor and a capacitor in parallel to extract the effective capacitance, which was calculated from the equation $C = 1/(2\pi f Im(Z))$ and where f is the frequency and Z is the measured impedance.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was partially supported by the Advanced Functional Materials Center at Linköping University and the Önnesjö Foundation. Authors wish to thank also the Knut and Alice Wallenberg Foundation (Power Paper project, scholars), VINNOVA, and STEM, the Swedish Energy Agency for financial support.

Received: July 9, 2014
Revised: August 29, 2014
Published online: October 6, 2014

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